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APPLICATION NO.	NO. FILING DATE FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,951	09/30/2003	Yukio Arima	SUSU121795	5298
7	590 03/01/2006	EXAMINER		
	D'Connor Johnson & K	TRIMMINGS, JOHN P		
Suite 2800 1420 Fifth Ave	enue		ART UNIT	PAPER NUMBER
Seattle, WA		2138		
			DATE MAN ED 02/01/000	_

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.		Applicant(s)					
Office Action Summer:		10/674,95	1	ARIMA ET AL.					
Office Action Summary			Examiner		Art Unit				
			John P. Tri	_	2138				
Period fo	The MAILING DATE of this communic or Reply	ation appe	ears on the	cover sheet with the c	correspondence ac	ldress			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).									
Status									
1)⊠	Responsive to communication(s) filed	l on 30 Se	ptember 2	003.					
·	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.								
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
4)⊠	4)⊠ Claim(s) <u>1-15</u> is/are pending in the application.								
	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)	5) Claim(s) is/are allowed.								
6)⊠	D⊠ Claim(s) <u>1-4,6-12,14 and 15</u> is/are rejected.								
7) 🖂	☑ Claim(s) <u>1-15</u> is/are objected to.								
8)[	8) Claim(s) are subject to restriction and/or election requirement.								
Applicati	on Papers								
9)⊠ The specification is objected to by the Examiner.									
10)⊠ The drawing(s) filed on <u>30 September 2003</u> is/are: a) accepted or b)⊠ objected to by the Examiner.									
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority u	ınder 35 U.S.C. § 119								
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)⊠ All b)□ Some * c)□ None of:									
	1. Certified copies of the priority documents have been received.								
<ul> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage</li> </ul>									
	application from the International Bureau (PCT Rule 17.2(a)).								
* See the attached detailed Office action for a list of the certified copies not received.									
				·					
Attachment	t(s)								
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)									
	e of Draftsperson's Patent Drawing Review (PT			Paper No(s)/Mail Da  5) Notice of Informal P	ail Date nal Patent Application (PTO-152)				
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  Paper No(s)/Mail Date  5) Notice of Informal Patent Application (PTO-152)  6) Other:									

#### **DETAILED ACTION**

Claims 1-15 are presented for examination.

#### **Priority**

1. The examiner acknowledges receipt of the applicant's claim of foreign priority based on an application filed 10/02/2002. The examiner may not be required to apply the foreign priority date to any rejections in this or any other office action because an English language translation has not been provided.

Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

#### Drawings

2. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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Art Unit: 2138

# Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

# Claim Objections

4. Claims 1-15 are objected to because of the following informalities:

As per Claim 1:

Line 8 should be corrected to recite, "... a save data storage unit which stores the save data ...".

As per Claims 2-7:

In the interest of clarity, the examiner requests that the 1<sup>st</sup> line of each claim recite, "A <u>The</u> device according to claim 1, ...".

As per Claim 8:

....

Line 3 should be corrected to recite, "... forming a scan chain, wherein the functional module ...".

Line 5 should be corrected to recite, "... a shift operation using the scan chain

Line 8 should be corrected to recite, "... a shift operation using the scan chain ...".

Line 24 should be corrected to recite, "... using the scan chain ...".

Line 28 should be corrected to recite, "... using the scan chain ...".

Line 34 should be corrected to recite, "... using the scan chain ...".

As per Claims 9-15:

In the interest of clarity, the examiner requests that the 1<sup>st</sup> line of each claim recite, "A <u>The</u> device according to claim 8, ...".

Appropriate correction is requested.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1, 2, 6-8, 10, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and further in view of Purdham, U.S. Patent No. 5701313. As per Claim 1:

Woods teaches an integrated circuit device comprising: at least one functional module (FIG.1 130) which outputs save data (FIG.2 234) in synchronism with a saving clock signal (see Claim 4 and paragraphs [0082 - 0090]); a power supply control unit (FIG.2 ISPRM 160) which selects one of the functional modules (one module is default thus selection is obvious), and controls stop and resumption of power supply (FIG.1 264) to the selected functional module (i.e., one default module); a save data storage unit (FIG.2 270) which stores save data output from a functional module (via FIG.2 268)

selected by the power supply control unit (FIG.2 260), but fails to further disclose error correction. The APA, on page 5 and 6, discloses inherent problems within the power conservation art, where there is an increased likelihood of "soft errors" occurring during "sleep mode". Page 6 lines 10-16 of the APA state a desirable attribute in the prior art to be the capability of minimizing the soft error problem. In the analogous art of Purdham, it is disclosed that soft errors are corrected in a transparent manner in order to minimize "soft errors" (see column 1 lines 37-50). Purdham discloses a memory containing an error checking and correction unit which performs error checking and correction for the save data stored in the save data storage unit when the save data is to be restored (see FIG. 5) to the functional module in synchronism with a restoration clock signal. Since the correction in Purdham is transparent to memory operation, it is obvious that the memory error checking and correction operations of Purdham will occur during restore clock operation (see Woods, Claim 4 and paragraphs [0082 - 0090]) to the functional module. One with ordinary skill in the art at the time of the invention, motivated as suggested above in the APA and Purdham, would have found it obvious to include error detection and correction (Purdham) to Woods in order to minimize soft error failure during sleep mode.

As per Claims 2 and 10:

Purdham further discloses the device according to claim 1 or 8, wherein the error checking and correction unit comprises: an encoder which generates an error correction code from the save data (FIG.5 236), and writes the error correction code in the save data storage unit (FIG.5 246); and a decoder (FIG.5 264) which reads out the stored

save data and the corresponding error correction code (FIG.5 250) from the save data storage unit, and decodes the save data (FIG.5 270). And in view of the motivation previously stated, the claims are rejected.

As per Claims 6 and 14:

Woods further teaches the device according to claim 1 or 8, which further comprises: a compressor which compresses the save data stored in the save data storage unit (paragraph [0071]); and an expander which expands the save data compressed by the compressor when the save data is to be restored to the functional module (this is an obvious and complementary component related to the compressor herein disclosed). And in view of the motivation previously stated, the claims are rejected.

As per Claims 7 and 15:

Woods further discloses the device according to claim 1, wherein the save data storage unit is a volatile memory (paragraphs [0017, 0057] and Claim 9). And in view of the motivation previously stated, the claims are rejected.

As per Claim 8:

Woods teaches an integrated circuit device comprising: at least one functional module (FIG.1 130) which has a plurality of flip-flops (paragraph [0030]) forming a scan chain (FIG.2 140), performs a saving operation by outputting data in the flip-flops by a shift operation using scan chain (paragraph [0056]) synchronized with a saving clock signal (see Claim 4 and paragraphs [0082 - 0090]), and performs a restoring operation by restoring, to the flip-flops, the saved data by a shift operation using scan chain

(paragraph [0088]) synchronized with a restoration clock signal (Claim 4); a power supply control unit (FIG.2 ISPRM 160) which selects one of the functional modules (one module is default thus selection is obvious), and controls stop and resumption of power supply (FIG.1 264) to the selected functional module (i.e., one default module); a clock signal generator (FIG.2 260 and Claim 4) which generates a saving clock signal and restoration clock signal (paragraphs [0051, 0056]) for the functional module (FIG.1 130) selected by the power supply control unit (default); a scan controller (FIG.2 260) which, in the saving operation or restoring operation (paragraphs [0083 – 0090]), sets the functional module selected by the power supply control unit to a scan test mode (FIG.2) 268), and selects the saving clock signal or restoration clock signal generated by the clock signal generator as a clock signal to be supplied for the shift operation using scan chain (Claim 4); a save data storage unit (FIG.2 270) which stores the save data output from the functional module (FIG.2 234) selected by the power supply control unit (via FIG.2 260) by the shift operation using scan chain synchronized with the saving clock signal (Claim 4) but fails to further disclose error correction. The APA, on page 5 and 6, discloses inherent problems within the power conservation art, where there is an increased likelihood of "soft errors" occurring during "sleep mode". Page 6 lines 10-16 of the APA state a desirable attribute in the prior art to be the capability of minimizing the soft error problem. In the analogous art of Purdham, it is disclosed that soft errors are corrected in a transparent manner in order to minimize "soft errors" (see column 1 lines 37-50). Purdham discloses a memory containing an error checking and correction unit which performs error checking and correction for the save data stored in the save data

storage unit when the save data is to be restored (see FIG. 5) to the functional module. Restoring is in synchronism with a restoration clock signal (Claim 4), to the flip-flops of the functional module by the shift operation using scan chain synchronized with the restoration clock signal Since the correction in Purdham is transparent to memory operation, it is obvious that the memory error checking and correction operations of Purdham will occur during restore clock operation (see Woods, Claim 4 and paragraphs [0082 - 0090]). One with ordinary skill in the art at the time of the invention, motivated as suggested above in the APA and Purdham, would have found it obvious to include error detection and correction (Purdham) to Woods in order to minimize soft error failure during sleep mode.

6. Claims 3, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and in view of Purdham, U.S. Patent No. 5701313 as applied to Claim 1, and further in view of Freeman et al. (herein Freeman), U.S. Patent No. 6510528.

As per Claim 3:

Where Woods and Purdham fail, Freeman teaches the device according to claim 1, wherein the error checking and correction unit periodically performs error checking and correction for the save data stored in the save data storage unit (see FIG.2). And the Background of Freeman states the advantage being a method of minimizing

memory failures during "sleep mode" by periodically correcting errors. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the periodic error correction of Freeman to the system of Woods and Purdham in order to maintain correct data in the save unit during sleep mode.

As per Claims 9 and 11:

Freeman further teaches the device according to claim 8, wherein the clock signal generator generates a clock signal for use in periodic error checking and correction performed in the save data storage unit (when changing state from S1 to S0 in FIG.2 of Freeman, the scrubbing routine causes memory readout that, in accordance with Purdham, corrects any data failures). The change of state and the scrubbing routine cause the test clock generator of Woods (Claim 4) to clock data out of the memory and into the functional module 130). And in view of the motivation previously stated, the claims are rejected.

7. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and in view of Purdham, U.S. Patent No. 5701313 as applied to Claim 1, and further in view of Smith III, U.S. Patent No. 5502728. Where Woods and Purdham fail, Smith III teaches the device according to claim 1 or 8, wherein the save data storage unit stores a plurality of copies of the save data, and the error checking and correction unit performs error checking and correction by a majority operation using said plurality

of copied data stored in the save data storage unit (FIG.5 51). And column 2 lines 36-51 state an advantage being improvement of data integrity of storage systems. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to add voter modeled data correction to the storage system of Woods and Purdham in order to improve data integrity.

## Allowable Subject Matter

8. Claims 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The references of Woods, Purdham, Smith III and Freeman fail to suggest or disclose the feature recited in the claims, wherein the save data storage unit is storage means for a built-in self-test circuit.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings

Examiner Art Unit 2138

jpt

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100